

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3444	"medium controller"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/06 17:59
L2	4	shared adj1 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/06 18:05
L3	10211	lock near8 status	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/06 18:05
L4	0	1 same 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/06 18:06
L5	16	1 and 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/06 18:06
L10	2	("6182196").URPN.	USPAT	OR	ON	2007/06/06 19:24
L11	5	("4928234" "5197130" "5450564" "5860159" "5920898").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/06/06 19:29
L12	2272	"shared storage"	US-PGPUB; USPAT; USOCR	OR	ON	2007/06/06 19:29
L13	11	1 and 12	US-PGPUB; USPAT; USOCR	OR	ON	2007/06/06 20:11
L14	786	1.clm.	US-PGPUB; USPAT; USOCR	OR	ON	2007/06/06 20:11
L15	366	12.clm.	US-PGPUB; USPAT; USOCR	OR	ON	2007/06/06 20:12

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L16	1	14 and 15	US-PGPUB; USPAT; USOCR	OR	ON	2007/06/06 20:13
L17	3934	execution near4 queue	US-PGPUB; USPAT; USOCR	OR	ON	2007/06/06 20:13
L18	694	17.clm.	US-PGPUB; USPAT; USOCR	OR	ON	2007/06/06 20:14
L19	6	1 and 18	US-PGPUB; USPAT; USOCR	OR	ON	2007/06/06 20:14
L20	11	12 and 18	US-PGPUB; USPAT; USOCR	OR	ON	2007/06/06 20:15



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1 [A system for computer music performance](#)



David P. Anderson, Ron Kuivila

February 1990 **ACM Transactions on Computer Systems (TOCS)**, Volume 8 Issue 1

Publisher: ACM Press

Full text available: pdf(2.21 MB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

A computer music performance system (CMPS) is a computer system connected to input devices (including musical keyboards or other instruments) and to graphic and audio output devices. A human performer generates input events using the input devices. The CMPS responds to these events by computing and performing sequences of output actions whose intended timing is determined algorithmically. Because of the need for accurate timing of output actions, the scheduling requirements of a CMPS differ ...

2 [The SuperSwift realtime executive: an astonishingly elegant solution to an age old problem](#)



Michel A. Lortie, J. Scott MacKay

July 1989 **Proceedings of the sixth Washington Ada symposium on Ada WADAS '89**

Publisher: ACM Press

Full text available: pdf(744.68 KB)

 Additional Information: [full citation](#), [index terms](#)

3 [Minerva: An automated resource provisioning tool for large-scale storage systems](#)


 Guillermo A. Alvarez, Elizabeth Borowsky, Susie Go, Theodore H. Romer, Ralph Becker-Szendy, Richard Golding, Arif Merchant, Mirjana Spasojevic, Alistair Veitch, John Wilkes
 November 2001 **ACM Transactions on Computer Systems (TOCS)**, Volume 19 Issue 4

Publisher: ACM Press

Full text available: pdf(701.98 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Enterprise-scale storage systems, which can contain hundreds of host computers and storage devices and up to tens of thousands of disks and logical volumes, are difficult to design. The volume of choices that need to be made is massive, and many choices have unforeseen interactions. Storage system design is tedious and complicated to do by hand, usually leading to solutions that are grossly over-provisioned, substantially under-performing or, in the worst case, both. To solve the configuration ni ...

Keywords: Disk array, RAID, automatic design

4 A survey of processors with explicit multithreading ☐



Theo Ungerer, Borut Robič, Jurij Šilc

March 2003 **ACM Computing Surveys (CSUR)**, Volume 35 Issue 1

Publisher: ACM Press

Full text available:  pdf(920.16 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Hardware multithreading is becoming a generally applied technique in the next generation of microprocessors. Several multithreaded processors are announced by industry or already into production in the areas of high-performance microprocessors, media, and network processors. A multithreaded processor is able to pursue two or more threads of control in parallel within the processor pipeline. The contexts of two or more threads of control are often stored in separate on-chip register sets. Unused i ...

Keywords: Blocked multithreading, interleaved multithreading, simultaneous multithreading

5 Fault-tolerant task management and load re-distribution on massively parallel hypercube systems ☐

I. Ahmad, A. Ghafoor

December 1992 **Proceedings of the 1992 ACM/IEEE conference on Supercomputing Supercomputing '92**

Publisher: IEEE Computer Society Press

Full text available:  pdf(1.16 MB)

Additional Information: [full citation](#), [references](#), [index terms](#)

6 Hot topic: architectures and NoC (4G wireless special day): Energy efficiency vs. programmability trade-off: architectures and design principles ☐

J. P. Robelly, H. Seidel, K. C. Chen, G. Fettweis

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**

Publisher: European Design and Automation Association

Full text available:  pdf(132.88 KB)

Additional Information: [full citation](#), [abstract](#), [references](#)

Performance achievements on programmable architectures due to process technology are reaching their limits, since designs are becoming wire- and power-limited rather than device limited. Likewise, traditional exploitation of instruction level parallelism saturates as the conventional approach for designing wider issue machines leads to very expensive interconnections, big instruction memory footprint and high register file pressure. New architectural concepts targeted to the application domain o ...

7 A simulation model for information system design, evaluation and planning ☐

Thomas G. DeLutis, Keith B. Johnston, James E. Rush, Patrick M.K. Wong

March 1979 **Proceedings of the 12th annual symposium on Simulation ANSS '79**

Publisher: IEEE Press

Full text available:  pdf(1.06 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this research, the use of simulation as a tool in information system design, evaluation and planning is being investigated. The modeled system is the on-line, real-time Computerized Library System of OCLC, Inc. Important characteristics of the OCLC System are described to establish a framework for discussion of the modeling and simulation

research which is the subject of this paper.

8 The LDF 100: a large grain dataflow parallel processor



Ian Kaplan

July 1987 **ACM SIGARCH Computer Architecture News**, Volume 15 Issue 3

Publisher: ACM Press

Full text available: pdf(665.04 KB) Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

The LDF 100 is a large grain dataflow parallel processor. The systems is designed to be incrementally expandable from 10 to over 128 processing elements. To avoid memory contention or prohibitive cost, the LDF 100 uses a distributed memory architecture. The LDF 100 also supports parallelism in the processing element. Each processing element consists of two microprocessors. One microprocessor is responsible for collecting data from the dataflow bus and one microprocessor is responsible for applic ...

9 Workload-ahead-driven online energy minimization techniques for battery-powered embedded systems with time-constraints



Yuan Cai, Marcus T. Schmitz, Bashir M. Al-Hashimi, Sudhakar M. Reddy

January 2007 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 12 Issue 1

Publisher: ACM Press

Full text available: pdf(370.69 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This article proposes a new online voltage scaling (VS) technique for battery-powered embedded systems with real-time constraints. The VS technique takes into account the execution times and discharge currents of tasks to further reduce the battery charge consumption when compared to the recently reported slack forwarding technique [Ahmed and Chakrabarti 2004], while maintaining low online complexity of $O(1)$. Furthermore, we investigate the impact of online rescheduling and remapping on t ...

Keywords: Dynamic voltage scaling, adaptive body biasing, battery, embedded systems

10 A semi distributed task allocation strategy for large hypercube supercomputers



Ishfaq Ahmad, Arif Ghafoor

November 1990 **Proceedings of the 1990 ACM/IEEE conference on Supercomputing Supercomputing '90**

Publisher: IEEE Computer Society

Full text available: pdf(1.27 MB) Additional Information: [full citation](#), [abstract](#), [references](#)

This paper presents a semi distributed approach for task scheduling in large parallel and distributed systems which is different from the conventional centralized and fully distributed approaches. The proposed strategy partitions the system into independent regions (spheres) centered at some control points. The central points called schedulers, optimally schedule tasks within their spheres and maintain state information with low overhead. We consider Hypercube systems for evaluation and using it ...

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 David Lammers. *Electronic Engineering Times*. Manhasset: May 23, 2005. ; p. 44 (1 page)

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 Robert Keenan. *Electronic Engineering Times*. Manhasset: Nov 18, 2002. ; p. 39 (1 page)

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 M2 Presswire. Coventry: Sep 17, 2001. ; p. 1

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 Business Editors & High-Tech Writers. *Business Wire*. New York: Nov 20, 2000. ; p. 1

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I FINDLETON, X ZHOU, G SASTRI - WO Patent WO/2005/048,131, 2005 - wipo.org

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